

EXPRESS MAIL LABEL
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5 **OPERATING TECHNIQUES FOR REDUCING PROGRAM AND READ
 DISTURBS OF A NON-VOLATILE MEMORY**

ABSTRACT OF THE DISCLOSURE

10 The present invention presents a non-volatile memory having a plurality of erase
 units or blocks, where each block is divided into a plurality of parts sharing the same
 word lines to save on the row decoder area, but which can be read or programmed
 independently. An exemplary embodiment is a Flash EEPROM memory with a NAND
 architecture that has blocks composed of a left half and a right half, where each part will
15 accommodate one or more standard page (data transfer unit) sizes of 512 bytes of data. In
 the exemplary embodiment, the left and right portions of a block each have separate
 source lines, and separate sets of source and drain select lines. During the programming
 or reading of the left side, as an example, the right side can be biased to produce channel
 boosting to reduce data disturbs. In an alternate set of embodiments, the parts can have
20 separate well structures.